A76

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 387 834 A2**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **90104813.2**

(22) Date of filing: **14.03.90**

(51) Int. Cl.5: **H01L 21/82, H01L 27/02, H01L 23/522**

The title of the invention has been amended (Guidelines for Examination in the EPO, A-III, 7.3).

(30) Priority: **14.03.89 JP 61559/89**

(43) Date of publication of application: **19.09.90 Bulletin 90/38**

(84) Designated Contracting States: **DE FR GB**

(71) Applicant: **KABUSHIKI KAISHA TOSHIBA**
72, Horikawa-cho Saiwai-ku
Kawasaki-shi Kanagawa-ken Tokyo(JP)

(72) Inventor: **Wada, Masashi**
6-408, 262-32, Kamigo-Cho, Sakae-Ku
Yokohama-Shi, Kanagawa-ken(JP)

(74) Representative: **Lehn, Werner, Dipl.-Ing. et al**
Hoffmann, Eitle & Partner Patentanwälte
Arabellastrasse 4
D-8000 München 81(DE)

(54) Semiconductor structure for processing and storing of information.

(57) A semiconductor device has a first functional block (202) for performing data processing and a second functional block (206, 302) for storing various information necessary for performing the data processing. The first functional block and a functional element section of the second functional block are directly formed on the semiconductor substrate (100). A memory cell array of the second functional block is formed above the first functional block and the like with a passivation film (110) interposed therebetween. The memory cell array has conductive wires (112) in the X direction and conductive wires (115) in the Y direction. The conductive wires in the X and Y directions are previously made conductive at optional three-dimensional intersections therebetween to thus form a mask ROM. An insulating film which is destroyed upon the application of a voltage is formed at the three-dimensional intersections to thus form a PROM. A ferroelectric member (117) which is polarized in accordance with an applied voltage direction is formed at the three-dimensional intersections to thus form an EEPROM.

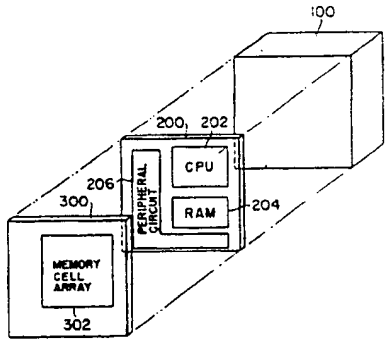

FIG. 1

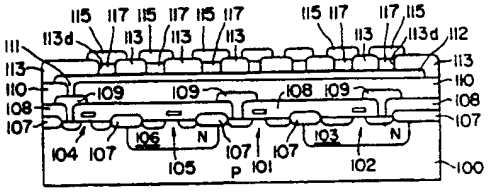

FIG. 5

EP 0 387 834 A2

SEMICONDUCTOR DEVICE

FIELD OF THE INVENTION

The present invention relates to a semiconductor device formed on a semiconductor substrate, and more particularly to a semiconductor device wherein elements for processing information and elements for storing information are formed on a single semiconductor substrate.

BACKGROUND OF THE INVENTION

With recent developments in semiconductor technology, a semiconductor device have been practically realized which has a great number of functional elements formed on a single semiconductor substrate. For example, there has been realized a semiconductor device having within its semiconductor substrate a CPU (Central Processing Unit) for performing logical operations, data control and the like, a ROM (Read Only Memory) for storing fixed data such as operating system (OS) and the like, a RAM (Random Access Memory) for storing temporary data, and other elements. Such a semiconductor device includes almost all functional elements necessary for a computer in one chip. A very compact device with great information processing capability is thus realized and has wide application to such as IC cards.

Such a semiconductor device has been desired to have a more sophisticated function as its memory capacity increases and its logical circuits become large scaled. The reason for this is that devices which can process more information at higher speeds are becoming necessary. In order to meet such requirements, it is necessary to integrate elements as much as possible on a single semiconductor substrate. It therefore becomes necessary to make each element smaller. If not possible, the chip area will increase to pose a number of problems associated with manufacturing techniques, resulting in a difficulty in mass-producing devices of low cost.

In order to make an element small, a precise control of lithography should be ensured and measures to count a degradation of reliability to be caused by miniaturization should be taken, thereby resulting in a difficulty associated with manufacturing techniques.

SUMMARY OF THE INVENTION

The present invention has been made in consideration of the above problems. It is an object of the present invention to provide a semiconductor device having both a large memory capacity and a highly sophisticated information processing capability and being formed on a single semiconductor substrate without any increase of the chip area and without the need of severe miniaturization of elements.

There are laminated, as an upper layer and lower layer on a single semiconductor substrate, a first functional block for data processing and a memory cell array of a second functional block for storage of various information necessary for the data processing. The overall dimensions of the semiconductor device can be made small when compared with a device which forms both the first and second functional blocks on the same surface. The miniaturization of the semiconductor device can be achieved without reducing the size of each of semiconductor elements constituting the first and second functional blocks small. There is no need therefore to miniaturize each semiconductor element, and hence there is no fear of lowering the reliability which might be caused by miniaturization.

According to the present invention, the information necessary for the data processing by the first functional block is previously stored in the memory cell array.

According to the present invention, virtual intersections (three-dimensional intersections) between conductive wires in the X- and Y-directions are optionally made conductive, or the state of ferroelectric members at virtual intersections is optionally changed. Accordingly, the information necessary for the data processing by the first functional block can be previously stored in the memory cell array of the second functional block. In other words, the information necessary for a particular user of this device can be previously stored in the memory cell array.

According to the present invention, the overall dimensions of a semiconductor device can be made small without reducing the size of each semiconductor element small. In addition, since it is not necessary to make each element small, the difficulty in manufacturing is not increased, thereby not only allowing devices of low cost but also presenting no fear of lowering the reliability which might be caused through miniaturization. Furthermore, the memory capacity can be increased and the data processing functions can be highly sophisticated assuming that a device having the same

dimensions as a conventional one is used.

According to the present invention, the information necessary for the data processing can be previously stored in the memory cell array.

According to the present invention, a user can optionally store in the memory cell the information necessary for the data processing, and in addition, information once stored can be rewritten.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic view illustrating the concept of the present invention;

Figs. 2A to 2C are cross sections illustrating the manufacturing processes of a semiconductor device according to an embodiment of the present invention;

Fig. 3 is a schematic view illustrating first and second wirings shown in Fig. 2C; and

Figs. 4 and 5 are cross sections of semiconductor devices according to other embodiments of this invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The embodiments of the present invention will be described with reference to the accompanying drawings.

Fig. 1 is a schematic view illustrating the concept of the present invention. As seen from Fig. 1, the embodiment semiconductor device has a lower layer 200 and an upper layer 300 laminated one upon the other on a semiconductor substrate 100. The lower layer 200 includes a first functional block (data processing section) and a part (constructed of transistors) of a second functional block (memory section). The upper layer 300 includes the remaining part (not including transistors) of the second functional block. The first functional block has a function of performing logical operations, data control and the like, and is shown as a CPU 202 in Fig. 1. The second functional block is used for storing information, a part of the first functional block being shown in Fig. 1 as a memory cell array 302 of ROM in the upper layer 300 and a RAM 204 and a peripheral circuit (decoder, control unit, input/output unit and the like) 206 of ROM in the lower layer 200.

Figs. 2A to 2C are cross sections illustrating the manufacturing processes of a semiconductor device according to the first embodiment which is an example of the device conceptually shown in Fig. 1.

The first embodiment operates as a mask ROM. As shown in Fig. 2A, there are formed on a semiconductor substrate (P-type silicon substrate) 100 an N-channel transistor 101 and P-channel transistor 102 as the data processing section. Reference numeral 103 represents an N-type well provided for the P-channel transistor 102. There are also formed on the surface of the silicon substrate 100 an N-channel transistor 104 and a P-channel transistor 105 which constitute the peripheral circuit of the memory section, e.g., a decoder, control unit, input/output unit and the like. Reference numeral 106 represents an N-type well provided for the P-channel transistor 105. These elements are electrically isolated from each other by field oxide 107, 107, ... Reference numeral 108 represents a passivation film deposited for protecting the elements, the passivation film being made of SiO_2 or PSG formed by a CVD method. Contact holes 108a, 108a, ... are formed in the passivation film 108 where necessary, and wiring material 109 is provided within the holes for interconnection between elements.

Next, as shown in Fig. 2B, a passivation film 110 is deposited on the passivation film 108 and wiring material 109. Contact holes 110a, 110a, ... are formed in the passivation film 110 for connection to the wirings of decoder outputs for the memory section, the contact holes 110a, 110a, ... being disposed as shown in Fig. 3 substantially in an L-character shape. Next, first metals (or semiconductor layers) 112, 112, ... are deposited in parallel with each other as shown in Fig. 3 while being connected to the wiring material 109 via the contact holes 110a, 110a, ...

Next, as shown in Fig. 2C, a passivation film 113 is deposited over the whole surface of the first metals 112 and passivation film 110. Contact holes 113a, 113a, ... are formed in the passivation film 113 above the first wirings 112 in accordance with the information to be written in ROMs. As seen from Fig. 3, the contact holes are selectively formed at optional virtual or apparent intersections (three-dimensional intersections as viewed in the direction perpendicular to the X-Y surface) between the first and second metals 112 and 115. Then, the second metals (or semiconductor layers) 115, 115, ... are deposited and patterned to be perpendicular to the first wirings as seen from Fig. 3. The end portions of the second metals are connected to the decoder outputs via the contact holes 110a, 110a, ... The interface at which the first and second metals (or semiconductor layers) contact each other within the contact holes 113a is formed with a p-n junction or Schottky junction so as to present a rectification function.

The semiconductor device constructed as above operates as described in the following. Namely, the transistor type functional elements

(data processing section) formed on the surface of the semiconductor substrate 100 perform information processing. Fixed information is being stored in the memory cell array formed above the transistor type functional elements, and is read when necessary.

As seen from Fig. 2C, without increasing the chip area, it is possible to realize a semiconductor device having a highly sophisticated information processing capability and a large memory capacity.

In the above embodiment, the data processing section and the peripheral circuit of the memory section have been formed on the surface of the semiconductor substrate 100. Other memories such as RAMs also may be formed on the surface of the substrate 100.

Another embodiment will be described with reference to Fig. 4 which shows a semiconductor device functioning as a PROM. In the first embodiment shown in Figs. 2A to 2C, contact holes 113a have been formed at the virtual intersections (three-dimensional intersections) between the first and second metals (or semiconductor layers) in accordance with information to be stored. In the second embodiment shown in Fig. 4, blind holes 113b, 113b are formed at all virtual intersections as shown in Fig. 4 while thin insulating films 113c, 113c, ... are interposed between two metals 112 and 115.

In order to form such blind holes, there are many practical methods. For example, holes 113b are first formed to extend completely to the first metal 112, and then an insulating film is deposited over the whole surface of the semiconductor device. Alternatively, the surface of the first metal 112, exposed to the holes 113b, may be oxidized.

In writing information into the semiconductor device shown in Fig. 4, the thin insulating films 113c, 113c are selectively destroyed for example by applying a high voltage pulse (10 MV/cm). It is therefore possible for a user to write a desired program into a finished semiconductor device, thereby realizing a so-called PROM type semiconductor device.

A further embodiment of this invention will be described with reference to Fig. 5 which shows a semiconductor device functioning as an EEPROM. In the embodiment shown in Fig. 4, a PROM type semiconductor device has been realized by forming a thin insulating film 113c at the virtual intersections between the first and second metals (or semiconductor layers) 112 and 115. In the embodiment shown in Fig. 5, ferroelectric members 117, 117, ... are formed in holes 113d, 113d, ... at virtual intersections. In practice, a ferroelectric member 117 may be deposited over the whole area of the semiconductor device inclusive of the holes 113d, and thereafter the film is etched back. Or other suitable methods may be used. As the ferroelectric member 117, barium titanate ($BaTiO_3$), lead titanate zirconate (PZT: $PbTiO_3$-$PbZrO_3$) or the like may be used.

In the semiconductor device shown in Fig. 5, a high voltage is selectively applied to the intersections to thereby change the polarization direction of the ferroelectric member 117 and store information. In other words, the semiconductor device shown in Fig. 5 functions as a non-volatile RAM (EEPROM).

Reference signs in the claims are intended for better understanding and shall not limit the scope.

Claims

1. A semiconductor device comprising:
a semiconductor substrate (100);
a first functional block (202) formed directly on said semiconductor substrate (100) for performing data processing;
a second functional block (206, 302) for previously storing information necessary for performing said data processing, said second functional block including a memory cell array (302) having a plurality of memory cells and a functional element section (206) at least for reading data from said memory cell array,
said functional element section being formed directly on said semiconductor substrate, and said memory cell array being formed above said first functional block and functional element section with an insulating passivation film (110) interposed therebetween.

2. A semiconductor device according to claim 1, wherein said first functional block is a CPU (202) and said second functional block is a mask ROM.

3. A semiconductor device according to claim 1, wherein said first functional block (202) formed directly on said semiconductor substrate (100) and said functional element section of said second functional block (206, 302) formed directly on said semiconductor substrate, each include a transistor.

4. A semiconductor device according to claim 1, wherein said memory cell array has a plurality of conductive wires (112) in the X direction and conductive wires (115) in the Y direction, respectively to be selected by a decoder, said conductive wires in the X and Y directions being formed as two upper and lower layers with an insulating film (113) interposed therebetween, and being three-dimensionally intersected.

5. A semiconductor device according to claim 4, wherein said second functional block is a mask ROM, wherein said conductive wires (112, 115) in the X and Y directions are electrically interconnected at optional three-dimensional intersections therebetween, in accordance with said information

to be previously stored.

6. A semiconductor device according to claim 4, wherein said second functional block is a PROM, wherein said conductive wires (112, 115) in the X and Y directions face each other at three-dimensional intersections therebetween with an insulating film (113c) interposed therebetween, said insulating film being destroyed and made electrically conductive by applying a voltage between said conductive wires in the X and Y directions forming said three-dimensional intersections.

7. A semiconductor device according to claim 6, wherein said voltage for destroying said insulating film (113c) has a value of applying more than 5 MV/cm in the direction of facing said conductive wires (112, 115) in the X and Y directions each other.

8. A semiconductor device according to claim 4, wherein said second functional block is an EEPROM, wherein said conductive wires (112, 115) in the X and Y directions face each other at three-dimensional intersections with a ferroelectric member (117) interposed therebetween, said ferroelectric member being polarized in the direction of a voltage which is applied between said conductive wires in the X and Y directions forming said three-dimensional intersections.

9. A semiconductor device according to claim 8, wherein said ferroelectric member (117) is barium titanate.

10. A semiconductor device according to claim 8, wherein said ferroelectric member (117) is lead titanate zirconate (PZT: $PbTiO_3$-$PbZrO_3$).

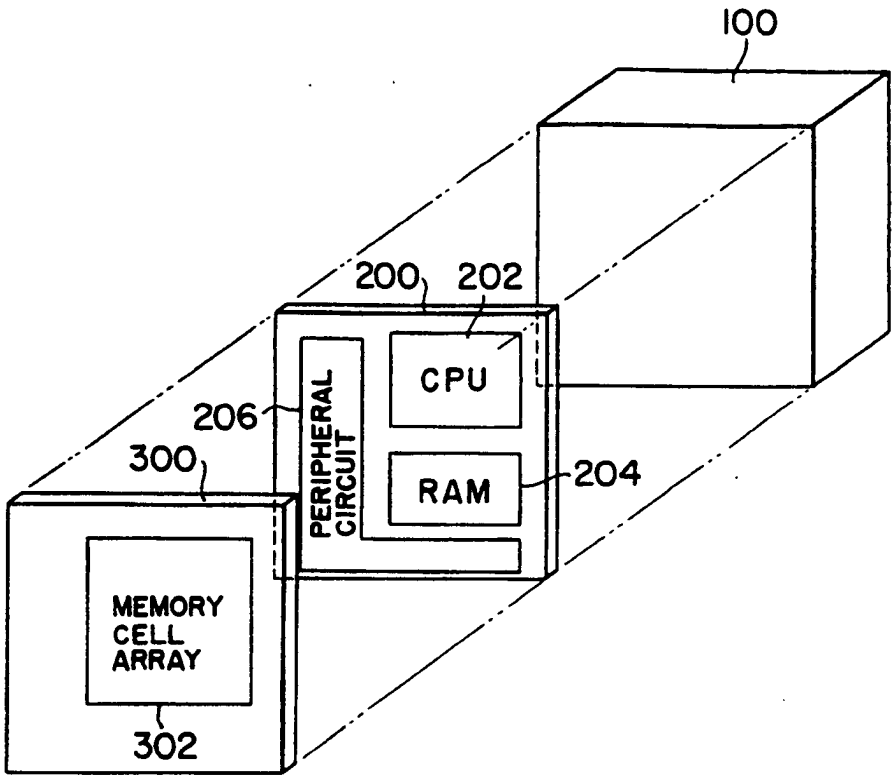
100
200
202
CPU
206
PERIPHERAL CIRCUIT
RAM
204
300
MEMORY CELL ARRAY
302

FIG. 1

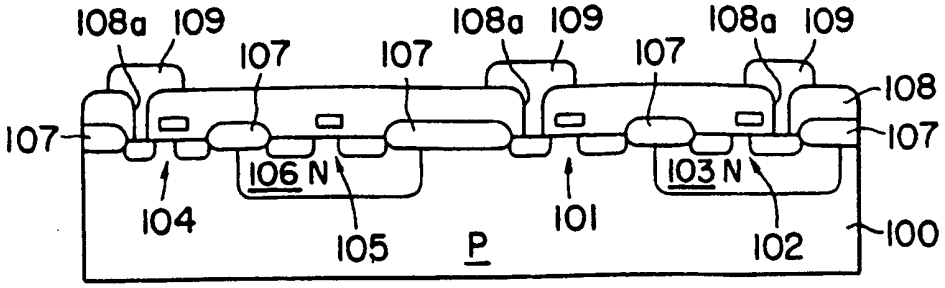

FIG. 2A

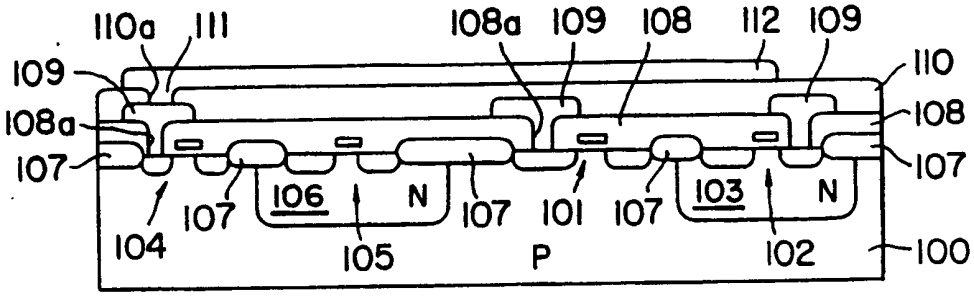

FIG. 2B

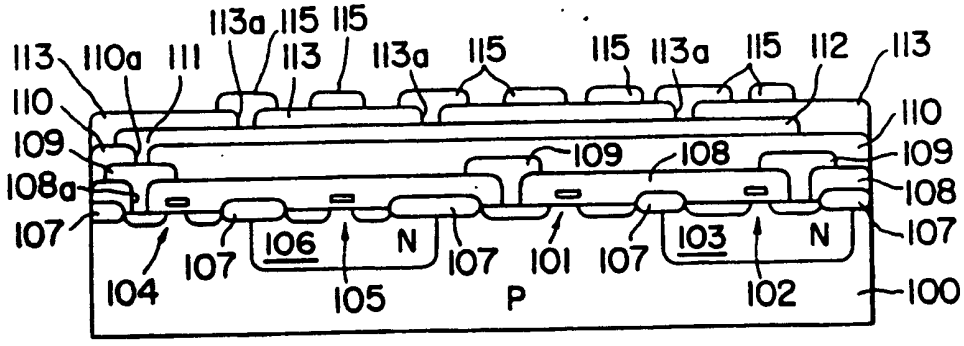

FIG. 2C

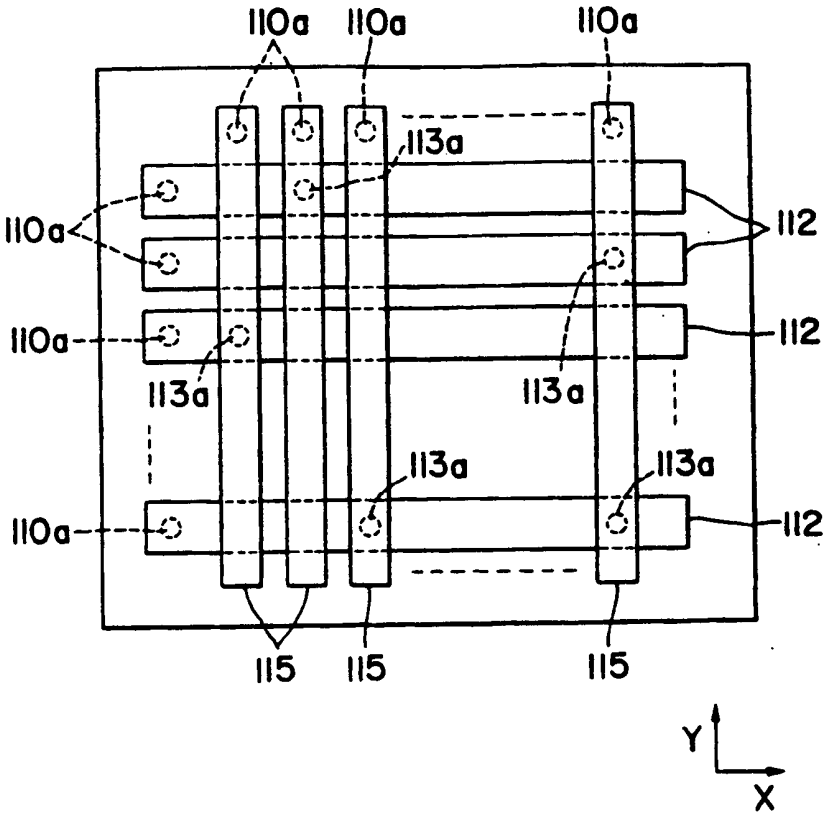
110a
110a
110a
113a
110a
112
112
110a
113a
113a
113a
113a
110a
112
115
115
115
Y
X

FIG. 3

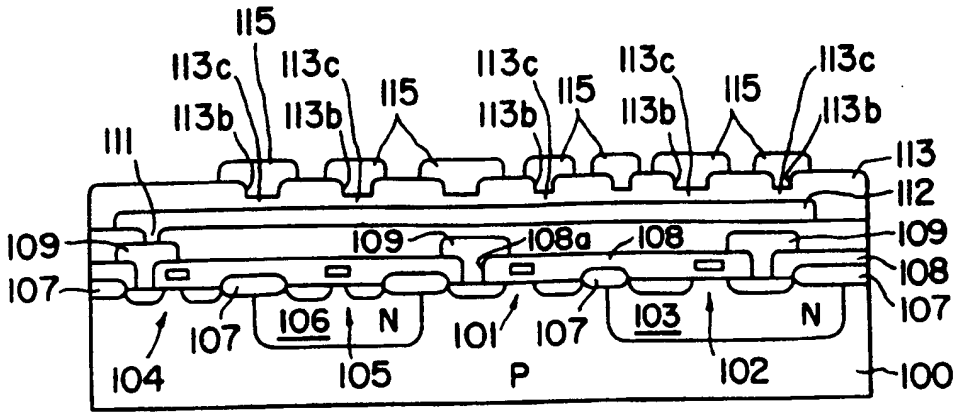
115
113c
113b
111
109
107
104
106
N
105
P
101
103
102
108a
108
112
113
100

FIG. 4

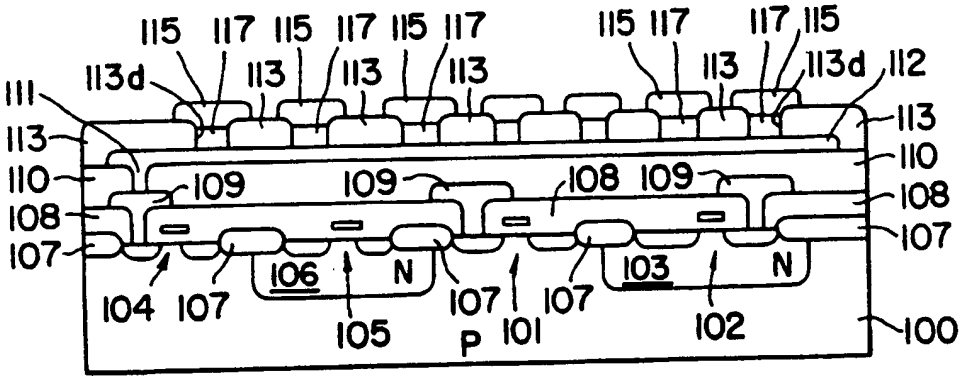
115
117
113
113d
111
110
109
108
107
104
106
N
105
P
101
103
102
112
100

FIG. 5